BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

Terms used
macro dyanmic library simulator electronic design algorithms

Found **70,574** of **137,188**

Sort results by: relevance

Display results: expanded form

Save results to a Binder

Search Tips

Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

Best 200 shown

Relevance scale

1 Power minimization in IC design: principles and applications

Massoud Pedram

January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1

Full text available: pdf(250.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies and techniques for designing low power digital CMOS circuits and systems and describes the many issues facing designers at architectural, logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy-delay product, gated clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, power management, power minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic simulation, synthesis, system design

2 Development of processors and communication networks for embedded systems: System design methodologies for a wireless security processing platform

Srivaths Ravi, Anand Raghunathan, Nachiketh Potlapally, Murugan Sankaradass

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(207.37 KB) Additional Information: full citation, abstract, references, citings, index terms

Security protocols are critical to enabling the growth of a wide range of wireless data services and applications. However, they impose a high computational burden that is mismatched with the modest processing capabilities and battery resources available on wireless clients. Bridging the security processing gap, while retaining sufficient programmability in order to support a wide range of current and future security protocol standards, requires the use of novel system architectures and design m ...

Keywords: 3DES, AES, DES, IPSec, RSA, SSL, decryption, design methodology, embedded system, encryption, handset, performance, platform, security, security processing, system

architecture, wireless

3 Regression-based RTL power modeling

Alessandro Bogliolo, Luca Benini, Giovanni De Micheli

July 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 3

Full text available: pdf(391.65 KB) Additional Information: full citation, abstract, references, citings, index terms

Register-transfer level (RTL) power estimation is a key feature for synthesis-based design flows. The main challenge in establishing a sound RTL power estimation methodology is the construction of accurate, yet efficient, models of the power dissipation of functional macros. Such models should be automatically built, and should produce reliable average power estimates. In this paper we propose a general methodology for building and tuning RTL power models. We address both hard macros (presy ...

Keywords: RTL design, RTL power modeling, adaptive characterization, functional macros, regression models

4 Formal verification in hardware design: a survey

Christoph Kern, Mark R. Greenstreet

April 1999 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 4 Issue 2

Full text available: pdf(411.53 KB) Additional Information: full citation, abstract, references, citings, index terms

In recent years, formal methods have emerged as an alternative approach to ensuring the quality and correctness of hardware designs, overcoming some of the limitations of traditional validation techniques such as simulation and testing. There are two main aspects to the application of formal methods in a design process: the formal framework used to specify desired properties of a design and the verification techniques and tools used to reason about the relationship between a spec ...

Keywords: case studies, formal methods, formal verification, hardware verification, language containment, model checking, survey, theorem proving

5 Fast detection of communication patterns in distributed executions

Thomas Kunz, Michiel F. H. Seuren

November 1997 **Proceedings of the 1997 conference of the Centre for Advanced Studies on Collaborative research**

Full text available: pdf(4.21 MB) Additional Information: full citation, abstract, references, index terms

Understanding distributed applications is a tedious and difficult task. Visualizations based on process-time diagrams are often used to obtain a better understanding of the execution of the application. The visualization tool we use is Poet, an event tracer developed at the University of Waterloo. However, these diagrams are often very complex and do not provide the user with the desired overview of the application. In our experience, such tools display repeated occurrences of non-trivial commun ...

6 Curriculum 68: Recommendations for academic programs in computer science: a report of the ACM curriculum committee on computer science

William F. Atchison, Samuel D. Conte, John W. Hamblen, Thomas E. Hull, Thomas A. Keenan, William B. Kehl, Edward J. McCluskey, Silvio O. Navarro, Werner C. Rheinboldt, Earl J. Schweppe, William Viavant, David M. Young

March 1968 **Communications of the ACM**, Volume 11 Issue 3

Full text available: pdf(6.63 MB) Additional Information: full citation, references, citings

Keywords: computer science academic programs, computer science bibliographies, computer science courses, computer science curriculum, computer science education, computer science graduate programs, computer science undergraduate programs

7 Design automation status in Japan

Akihiko Yamada

June 1981 **Proceedings of the eighteenth design automation conference on Design automation**

Full text available: pdf(515.38 KB) Additional Information: full citation, abstract, references, index terms

This paper surveys the Japanese design automation (DA) status and activities. First, the DA statistics for major Japanese organizations are presented. These statistics show the status of logic, physical and test DA for digital systems and LSIs. Second, notable DA activities of Japanese manufacturers, laboratories and universities are introduced.

8 Fast high-level power estimation for control-flow intensive design

Kamal S. Khouri, Ganesh Lakshminarayana, Niraj K. Jha

August 1998 **Proceedings of the 1998 international symposium on Low power electronics and design**

Full text available: pdf(901.04 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present a power estimation technique for control-flow intensive designs that is tailored towards driving iterative high-level synthesis systems, where hundreds of architectural trade-offs are explored and compared. Our method is fast and relatively accurate. The algorithm utilizes the behavioral information to extract branch probabilities, and uses these in conjunction with switching activity and circuit capacitance information, to estimate the power consumption of a given ...

9 Design automation of electronics in Sweden

Höglund I., Fransson L., Almen Å A., Magnhagen B., Kjelkerud E., Thessén O.

January 1975 **Proceedings of the 12th design automation conference**

Full text available: pdf(560.35 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the status of design automation of electronics in three different companies and a university in Sweden. Design automation of MOS circuits at Asea-Hafo (Ingmar Höglund) Asea-Hafo is a company, which produces high reliability semiconductor devices as integrated circuits, discrete transistors, diodes and opto electronic components. During 1974 CMOS Large scale integrated circuits has become the main product. Asea ...

10 An interactive design automation system

Stephen Y. H. Su

June 1973 **Proceedings of the tenth design automation workshop on Design automation**

Full text available: pdf(851.96 KB) Additional Information: full citation, abstract, references, citings, index terms

An interactive design automation system is presented which, after complete implementation, will allow the designer to check the determinacy and dead locks of the system before implementation. The design can be evaluated at various levels and modified

interactively. The designer enters his design specification using either graphical representation or design language statements. The translator accepts the input and produces a data base for both the simulator and the logic synthesizer. The syn ...

11 System-level power optimization: techniques and tools

Luca Benini, Giovanni de Micheli

April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2

Full text available: pdf(385.22 KB) Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

12 Efficient power co-estimation techniques for system-on-chip design

Marcello Lajolo, Anand Raghunathan, Sujit Dey

January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(124.92 KB) Publisher Site Additional Information: full citation, references, citings, index terms

13 A design automation system for electronic switching systems

T. Hosaka, K. Ueda, H. Matsuura

June 1981 **Proceedings of the eighteenth design automation conference on Design automation**

Full text available: pdf(417.01 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the development and operation experience of NTT's design automation (DA) system for analog/digital switching systems. The DA system is composed of several subsystems, such as logic design, physical design, documentation and manufacturing data conversion programs, organized around the centralized data base management system. By using this system, hardware standardization and products compatibility among different manufacturers have been achieved. Th ...

14 VAMP: a VHDL based concept for accurate modeling and post layout timing simulation of electronic systems

Bernhard Wunder, Gunther Lehmann, Klaus D. Müller-Glaser

June 1996 **Proceedings of the 33rd annual conference on Design automation conference**

Full text available: pdf(330.37 KB) Additional Information: full citation, references, citings, index terms

15 High level hierarchical fault simulation techniques

William A. Rogers, Jacob A. Abraham

March 1985 **Proceedings of the 1985 ACM thirteenth annual conference on Computer Science**

Full text available: pdf(1.06 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents techniques for simulating directly from a hierarchical circuit description

without flattening to the level of primitives. An overview of traditional fault simulation techniques is followed by details of the hierarchical techniques. The fault model is shown to be decoupled from the simulator programs through the use of a fault library. The fault library allows the user to mix both functional and technology-dependent fault models, which allows fault simulation and conseque ...

16 A recursive algorithm for low-power memory partitioning

Luca Benini, Alberto Macii, Massimo Poncino

August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**

Full text available: pdf(324.58 KB) Additional Information: full citation, abstract, references, citings, index terms

Memory-processor integration offers new opportunities for reducing the energy of a system. In the case of embedded systems, one solution consists of mapping the most frequently accessed addresses onto the on-chip SRAM to guarantee power and performance efficiency. This option is especially effective when memory access patterns can be profiled and studied at design time (as in typical real-time embedded systems).In this work, we propose an algorithm for the automatic partitioning ...

17 Philo-a VLSI design system

R. Donze, J. Sanders, M. Jenkins, G. Sporzynski

January 1982 **Proceedings of the nineteenth design automation conference**

Full text available: pdf(594.87 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a design system capable of designing chips in the range of 5K to 7K equivalent three-way NOR gates. A key feature of the system is the ability to design chips with large macros (RAMs and PLAs). This design system is part of IBM's corporate-wide Engineering Design System (EDS). EDS provides the capabilities of logic simulation, automatic placement and wiring, checking, and test pattern generation (I). This paper describes the key capabilities of the system, specifically ...

18 High-level software energy macro-modeling

T. K. Tan, A. K. Raghunathan, G. Lakishminarayana, N. K. Jha

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(205.86 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents an efficient and accurate high-level software energy estimation methodology using the concept of characterization-based macro-modeling. In characterization-based macro-modeling, a function or sub-routine is characterized using an accurate lower-level energy model of the target processor, to construct a macro-model that relates the energy consumed in the function under consideration to various parameters that can be easily observed or calculated from a high-level programm ...

19 Copy detection for intellectual property protection of VLSI designs

Andrew B. Kahng, Darko Kirovski, Stefanus Mantik, Miodrag Potkonjak, Jennifer L. Wong

November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(109.67 KB) Additional Information: full citation, abstract, references, citings, index terms

We give the first study of copy detection techniques for VLSI CAD applications; these techniques are complementary to previous watermarking-based IP protection methods in finding and proving improper use of design IP. After reviewing related literature (notably in the text processing domain), we propose a generic methodology for copy detection based

on determining basic elements within structural representations of solutions (IPs), calculating (context-independent) signatur ...

20 A semi-custom design flow in high-performance microprocessor design

Gregory A. Northrop, Pong-Fei Lu
June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(186.80 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we present techniques shown to significantly enhance the custom circuit design process typical of high-performance microprocessors. This methodology combines flexible custom circuit design with automated tuning and physical design tools to provide new opportunities to optimized design throughout the development cycle.

Keywords: circuit tuning, custom design, methodology, standard cell

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	492	electronic adj design adj automation	USPAT	2004/06/14 11:14
2	BRS	L2	677	electronic adj design adj automation	USPAT; DERWENT; IBM_TDB	2004/06/14 11:15
3	BRS	L3	1	L1 and (macros)and (dynamic adj link adj library)	USPAT; DERWENT; IBM_TDB	2004/06/14 11:22
4	BRS	L4	63	L1 and (macros)and library	USPAT; DERWENT; IBM_TDB	2004/06/14 11:23
5	BRS	L5	0	L1 and (macros)and library and alorithms	USPAT; DERWENT; IBM_TDB	2004/06/14 11:23
6	BRS	L6	41	L1 and (macros)and library and algorithms	USPAT; DERWENT; IBM_TDB	2004/06/14 11:30
7	BRS	L7	0	L1 and (macros)and library and algorithms and plug-ins	USPAT; DERWENT; IBM_TDB	2004/06/14 11:25
8	BRS	L8	0	L1 and (macros)and library and algorithms and plugins	USPAT; DERWENT; IBM_TDB	2004/06/14 11:26
9	BRS	L9	0	L1 and library and algorithms and (plurality near macros)	USPAT; DERWENT; IBM_TDB	2004/06/14 11:26

	Type	L #	Hits	Search Text	DBs	Time Stamp
10	BRS	L10	471	(plurality near macros)	USPAT; DERWENT; IBM_TDB	2004/06/14 11:26
11	BRS	L11	1	(plurality near macros) and L1	USPAT; DERWENT; IBM_TDB	2004/06/14 11:26
12	BRS	L12	15	L1 and (macros$)and library and algorithms	USPAT; DERWENT; IBM_TDB	2004/06/14 11:31
13	BRS	L13	0	L1 and (application near macro)and library and algorithms	USPAT; DERWENT; IBM_TDB	2004/06/14 11:32
14	BRS	L14	0	L1 and (many near macro)and library and algorithms	USPAT; DERWENT; IBM_TDB	2004/06/14 11:32
15	BRS	L15	1	L1 and (different near macro)and library and algorithms	USPAT; DERWENT; IBM_TDB	2004/06/14 11:37
16	BRS	L16	0	L1 and (different near macro)and (dll) and algorithms	USPAT; DERWENT; IBM_TDB	2004/06/14 11:37
17	BRS	L17	0	L1 and (different near macro)and (dyanamic adj link librariesl) and algorithms	USPAT; DERWENT; IBM_TDB	2004/06/14 11:38
18	BRS	L18	1	L1 and (different near macro)and (dyanamic adj link libraries) and algorithms	USPAT; DERWENT; IBM_TDB	2004/06/14 11:38

	Type	L #	Hits	Search Text	DBs	Time Stamp
19	BRS	L19	0	L1 and (different near macro)and (dyanamic adj link adj libraries) and algorithms	USPAT; DERWENT; IBM_TDB	2004/06/14 11:39
20	BRS	L20	0	L1 and (different near macro) and (Windows adj DDLs)	USPAT; DERWENT; IBM_TDB	2004/06/14 11:39
21	BRS	L21	2	(Windows adj DDLs)	USPAT; DERWENT; IBM_TDB	2004/06/14 11:45
22	BRS	L22	2	(Windows adj DDLs) and macros	USPAT; DERWENT; IBM_TDB	2004/06/14 11:45

	~~Comments~~	Error Definition	Errors
19			0
20			0
21			0
22			0

	Type	Hits	Search Text
1	BRS	492	electronic adj design adj automation
2	BRS	677	electronic adj design adj automation
3	BRS	1	(electronic adj design adj automation) and (macros)and (dynamic adj link adj library)
4	BRS	63	(electronic adj design adj automation) and (macros)and library
5	BRS	0	(electronic adj design adj automation) and (macros)and library and alorithms
6	BRS	41	(electronic adj design adj automation) and (macros)and library and algorithms
7	BRS	0	(electronic adj design adj automation) and (macros)and library and algorithms and plug-ins
8	BRS	0	(electronic adj design adj automation) and (macros)and library and algorithms and plugins
9	BRS	0	(electronic adj design adj automation) and library and algorithms and (plurality near macros)
10	BRS	471	(plurality near macros)
11	BRS	1	(plurality near macros) and (electronic adj design adj automation)
12	BRS	15	(electronic adj design adj automation) and (macros$)and library and algorithms
13	BRS	0	(electronic adj design adj automation) and (application near macro)and library and algorithms
14	BRS	0	(electronic adj design adj automation) and (many near macro)and library and algorithms
15	BRS	1	(electronic adj design adj automation) and (different near macro)and library and algorithms
16	BRS	0	(electronic adj design adj automation) and (different near macro)and (dll) and algorithms
17	BRS	0	(electronic adj design adj automation) and (different near macro)and (dyanamic adj link librariesl) and algorithms
18	BRS	1	(electronic adj design adj automation) and (different near macro)and (dyanamic adj link libraries) and algorithms
19	BRS	0	(electronic adj design adj automation) and (different near macro)and (dyanamic adj link adj libraries) and algorithms
20	BRS	0	(electronic adj design adj automation) and (different near macro) and (Windows adj DDLs)
21	BRS	2	(Windows adj DDLs)

	DBs	Time Stamp	Comments	Error Definition
1	USPAT	2004/06/14 11:14		
2	USPAT; DERWENT; IBM_TDB	2004/06/14 11:15		
3	USPAT; DERWENT; IBM_TDB	2004/06/14 11:22		
4	USPAT; DERWENT; IBM_TDB	2004/06/14 11:23		
5	USPAT; DERWENT; IBM_TDB	2004/06/14 11:23		
6	USPAT; DERWENT; IBM_TDB	2004/06/14 11:30		
7	USPAT; DERWENT; IBM_TDB	2004/06/14 11:25		
8	USPAT; DERWENT; IBM_TDB	2004/06/14 11:26		
9	USPAT; DERWENT; IBM_TDB	2004/06/14 11:26		
10	USPAT; DERWENT; IBM_TDB	2004/06/14 11:26		
11	USPAT; DERWENT; IBM_TDB	2004/06/14 11:26		
12	USPAT; DERWENT; IBM_TDB	2004/06/14 11:31		
13	USPAT; DERWENT; IBM_TDB	2004/06/14 11:32		
14	USPAT; DERWENT; IBM_TDB	2004/06/14 11:32		
15	USPAT; DERWENT; IBM_TDB	2004/06/14 11:37		
16	USPAT; DERWENT; IBM_TDB	2004/06/14 11:37		
17	USPAT; DERWENT; IBM_TDB	2004/06/14 11:38		
18	USPAT; DERWENT; IBM_TDB	2004/06/14 11:38		
19	USPAT; DERWENT; IBM_TDB	2004/06/14 11:39		
20	USPAT; DERWENT; IBM_TDB	2004/06/14 11:39		
21	USPAT; DERWENT; IBM_TDB	2004/06/14 11:45		

	Type	Hits	Search Text
22	BRS	2	(Windows adj DDLs) and macros

	DBs	Time Stamp	Comments	Error Definition
22	USPAT; DERWENT; IBM_TDB	2004/06/14 11:45		